

DDR5 Client PMIC on DIMM

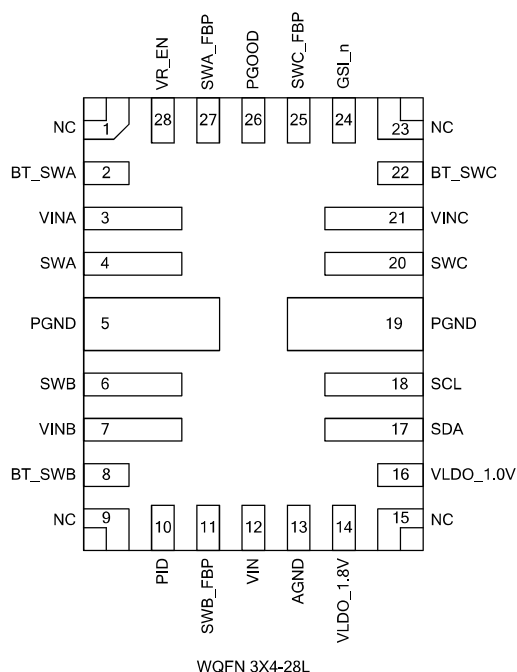
GENERAL DESCRIPTION

The PMD6805 PMIC is an integrated power management integrated circuit. It is optimized for DDR5 SO-DIMM/UDIMM application. The PMD6805 is highly flexible to be configured via I2C/I3C for multiple applications without PCB BOM changed.

The PMD6805 includes three DC/DC step down converters using integrated power FETs, two low-drop out regulators (LDOs). SWA and SWB can be configured as dual-phase converter. All converts use an asynchronous constant on-time, ACOT, control architecture to optimize the load transient response with smaller output capacitors. The LDOs only require small ceramic capacitors.

The PMD6805 PMIC is available in a 3x4 mm WQFN-28L package.

PIN CONFIGURATION



BENEFITS AND FEATURES

- **Input voltage range**
 - VIN = 4.25v to 5.5V
- **Completer Integrated Power Solution**
 - Programmable Dual Phase or Single Phase Converters for SWA and SWB
 - Single Phase Converter for SWC
 - Two LDOs for VOUT_1.8V and VOUT_1.0V
- **Space Savings**
 - Fully Integrated power FETs
 - Support Pure MLCC Output Capacitor
 - Power Sequencing Control by I2C/I3C Protocol
- **Easy System Level Design**
 - Configurable Sequencing
 - Programmable Frequency/Output Voltage for Each Power Rails
 - Programmable and DIMM Specific Registers for Customization
 - Programmable Diagnostic Mode for Debug and Validation
- **Complete Protection Mechanisms**
 - Input Voltage UVLO/OVP
 - Output Current Limit/OVP/UVF
 - Over Temperature Protection
 - Common ADC Channels
- **Highly Configurable**
 - General Status Interrupt (GSI) Function
 - VR_EN Function
 - Power Good Indicator
 - MTP Non-Volatile Memory (NVM)

I2C/I3C Interface

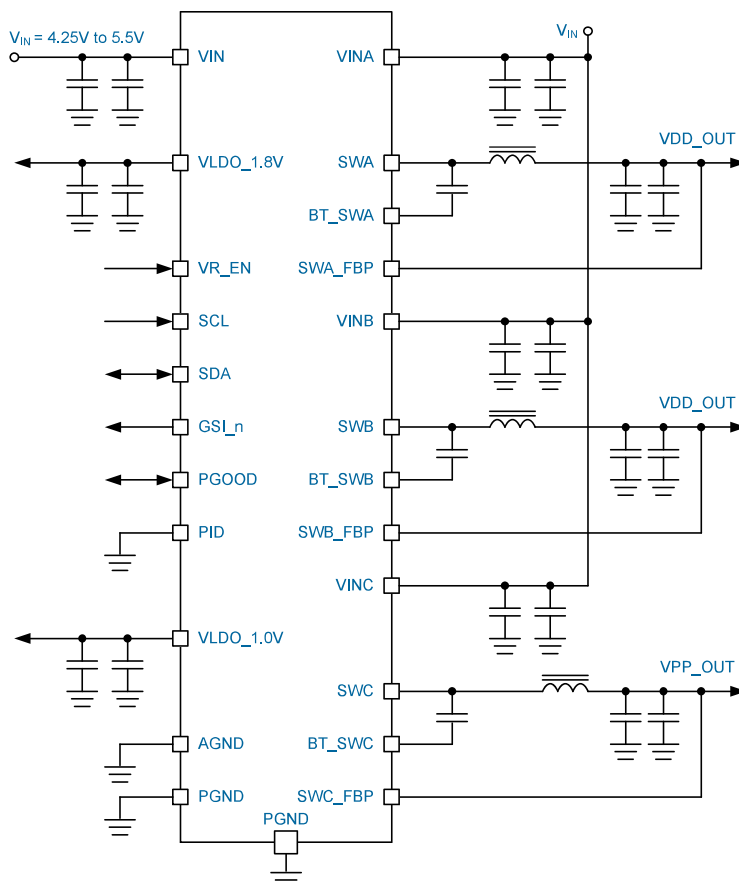
APPLICATIONS

- DDR5 SO-DIMM for NB/DT systems
- DDR5 UDIMM for DT systems

ORDERING INFORMATION

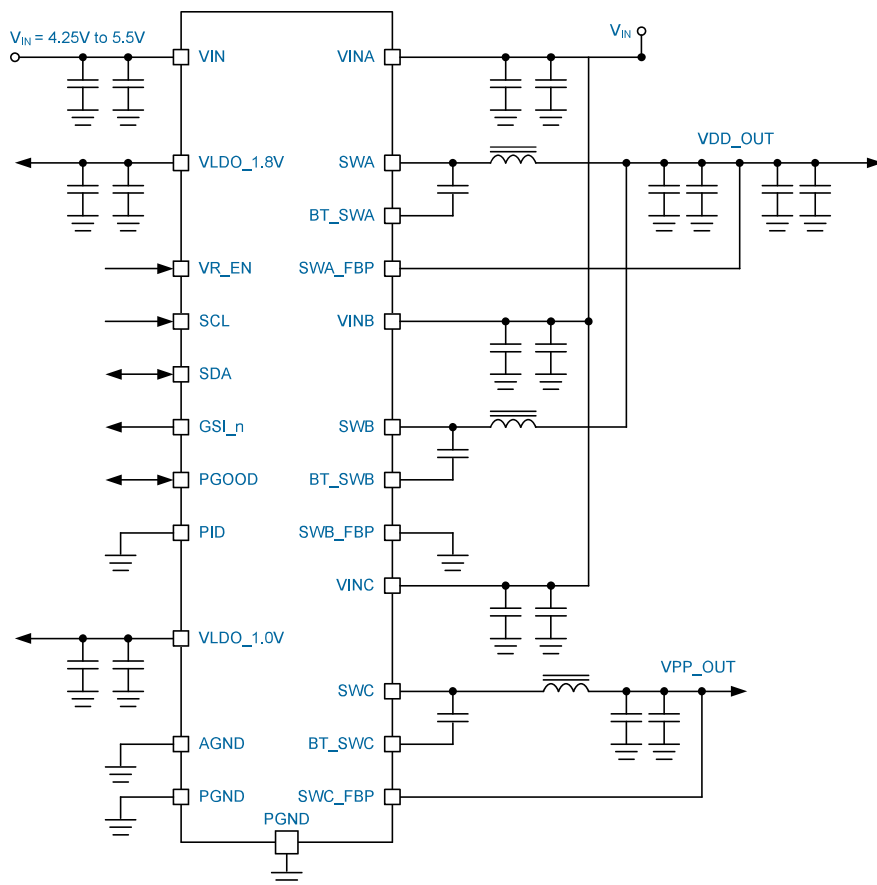
Part Number	Package
PMD6805AQ	WQFN-28L, 3.0x4.0

TYPICAL APPLICATION CIRCUIT



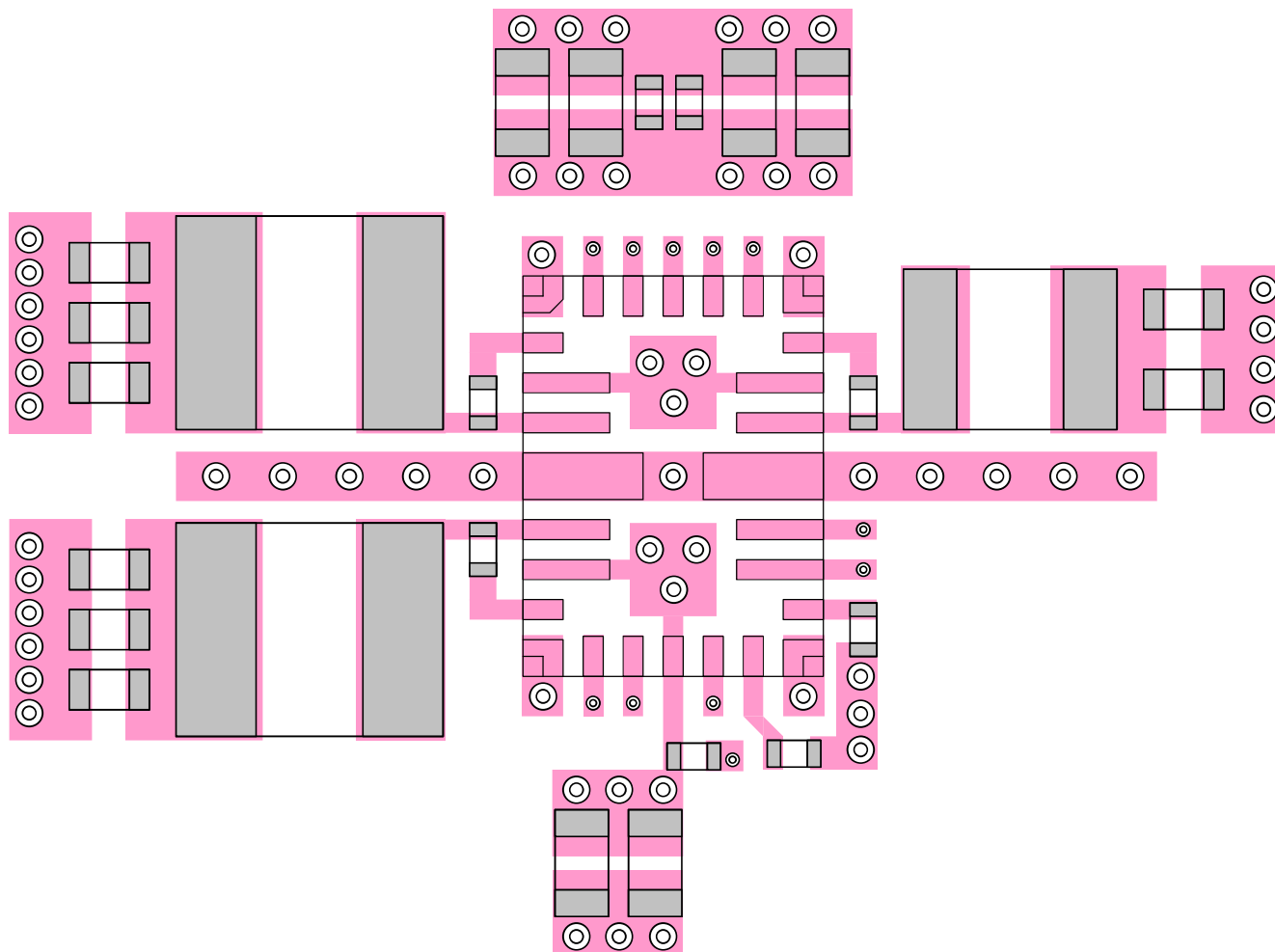
SWA and SWB are oprating in Single Phase Mode

TYPICAL APPLICATION CIRCUIT



SWA and SWB are combined as Dual Phase Mode

LAYOUT CONSIDERATION



- Input bypass capacitors must be closed to VIN and PGND pins to reduce the input current ripple which induced by switching operation.
- Power GND must be connected to a strong ground plane, Analog GND connect to PGND through via.
- Output inductor should be as close as possible to the PMIC to minimize lower power loss due to copper plane.
- The loop area of Inductor and output capacitor should be minimized in order to suppress generating switching noise.
- Place BT capacitor as close as possible to BT and SW pins of the PMIC to ensure clean and stable power.
- All sensitive analog traces and components should be placed away from high voltage switching components.

PACKAGE OUTLINE DRAWING

