

SPD HUB for DDR5 Memory Modules

BENEFITS AND FEATURES

- Two wire I2C or I3C Basic bus serial interface
- Single device load on the Host bus
- Up to 12.5 MHz transfer rate
- 1.8 V, 1.0 V power supply input
- 1.0V Push Pull I/O levels
- 1.0V, 1.1V, 1.2V, 1.8V, 2.5V, and 3.3V Open Drain IO levels
- 1024 Bytes of non-volatile memory (16 blocks; 64 bytes per block)
- Hub Function
- Integrated Temperature Sensor
- Packet Error Check (PEC) Function
- Parity Error Check Function
- Bus Reset Function
- Up to 8 unique addressing
- In Band Interrupt (IBI)
- Write protection for each block of NVM
- 9-pin thermally enhanced DFN package

APPLICATIONS

- DDR5 SO-DIMM/UDIMM for NB/DT systems
- DDR5 RDIMM/LRDIMM/NVDIMM for Server/Workstations

ORDERING INFORMATION

Part Number	Package
PMD5118ACD	DFN-8, 2.0x3.0

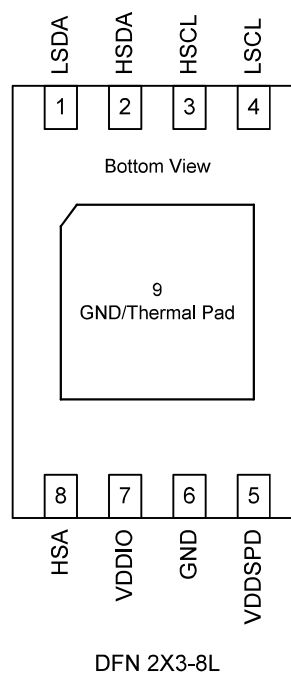
GENERAL DESCRIPTION

The SPD5 Hub device family contains 1024 bytes of non-volatile memory arranged as 16 blocks of 64 bytes per block. Each block may optionally be write protected via software command. Write protection for each block may be overridden in an offline programmer environment while overrides are prevented in normal use. The SPD5 Hub device operate from 1.8 V nominal power supply input. The SPD5 device is intended to operate up to 12.5MHz on a 1.0V I3C Basic IO bus or up to 1MHz on a 1.0V to 3.3V I2C IO bus. The SPD5 Hub devices are intended to interface to I2C/I3C Basic buses which have multiple devices on a shared bus, and must be uniquely soaddressed with fixed addressing on the same bus.

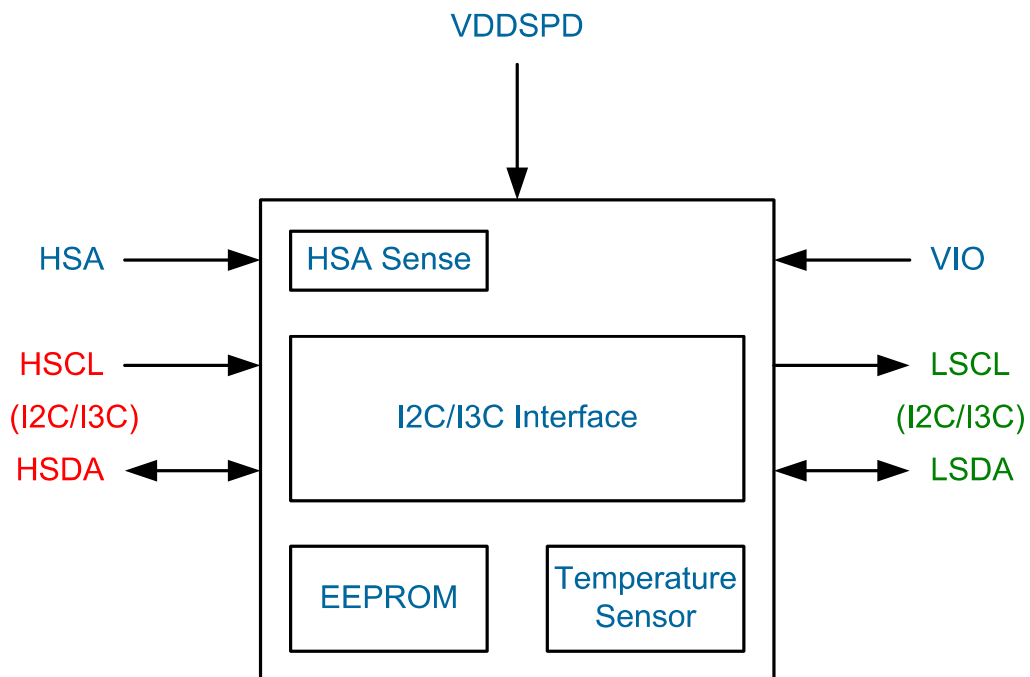
The PMD5118A device incorporates thermal sensing capability which is controlled and read over I2C/I3C Basic bus.

The PMD5118A is available in a 2x3 mm DFN-8L package.

PIN CONFIGURATION



BLOCK DIAGRAM



PACKAGE OUTLINE DRAWING

